Amendments to the Specification

Kindly amend the specification as follows:

Amend the title as:

A METHOD OF ENCAPSULATING CONDUCTIVE LINES OF SEMICONDUCTOR DEVICES ~~AND MANUFACTURING METHOD THEREOF~~

Page 1, between the title and the heading "**FIELD OF THE INVENTION**", insert

--CROSS REFERENCE TO RELATED APPLICATIONS

This is a divisional application of application Serial No. 09/616,378, filed July 13, 2000, which is hereby incorporated by reference in its entirety for all purposes.--

Please replace the paragraph beginning on page 1, line 8 with the following amended paragraph:

A chip on board (COB) is well known as a mounting structure which is fabricated without a molding [[die]] to reduce costs.

Please replace the paragraph beginning on page 1, line 10 with the following amended paragraph:

A conventional COB structure is shown in Fig. 7(A) and Fig. 7(B). Fig. 7(A) is a plane view of the COB structure and Fig. 7(B) is a cross section view along the line [[X-X']] 7B-7B shown in Fig. 7(A). In Fig. 7(A), an encapsulating material is not shown to facilitate understanding.

Please replace the paragraph beginning on page 5, line 3 with the following amended paragraph:

Fig. 1(B) is a cross section at a portion along line [[X-X']] 1B-1B shown in Fig. 1(A).

Please replace the paragraph beginning on page 5, line 6 with the following amended paragraph:

Fig. 2(B) is a cross section at a portion along line [[X-X']] 2B-2B shown in Fig. 2(A).

Please replace the paragraph beginning on page 5, line 16 with the following amended paragraph:

Fig. 7(B) is a cross section at a portion along line [[X-X']] 7B-7B shown in Fig. 7(A).

Please replace the paragraph beginning on page 6, line 6 with the following amended paragraph:

Fig. 1(A) is a plane view of a semiconductor device according to a first preferred embodiment of the present invention. Fig. 1(B) is a cross section view along line [[X-X']] 1B-1B shown in Fig. 1(A). In Fig. 1(A), an encapsulating material is not shown to facilitate understanding.

Please replace the paragraph beginning on page 9, line 5 with the following amended paragraph:

According to the first preferred embodiment, as the second wall 21 is located on the semiconductor chip 11, a space which is filled with the encapsulating material 22 becomes smaller. That is an interval L1 between the first wall 20 and the second wall 21 is shorter than an [[a]] interval L2 between opposing sides of wall 8 of the conventional device shown in Fig. 7(B). Therefore, as a surface tension becomes small, compared with the conventional device, a thickness of the central portion of the encapsulating material 22 is not made thin. That is, a uniformity of the surface of the encapsulating material 22 can be realized. As a result, the exposure of top portions 17a can be avoided. The shorter the interval L1, the smaller the surface tension. The interval L1 can be defined by a designer, based on a coefficient of viscosity of the encapsulating material, a height of the top portion of the conductive line and/or the size of the semiconductor device.

Please replace the paragraph beginning on page 11, line 3 with the following amended paragraph:

Fig. 2(A) is a plane view of a semiconductor device according to a second preferred embodiment of the present invention. Fig. 2(B) is a cross section view along line [[X-X']] 2B-2B shown in Fig. 2(A). In Fig. 2(A), an encapsulating material is not shown to facilitate understanding. In these ~~figure~~ figures, elements which correspond

to the elements of the first preferred embodiment are marked with the same symbols.

Please replace the paragraph beginning on page 13, line 14 with the following amended paragraph:

A method of manufacture according to a fourth embodiment will be shown hereinafter referring to Fig. 4(A)-Fig. 4(C). Fig. 5 is a plane view of a semiconductor device according to the fourth preferred embodiment of the present invention. Fig. 4(A)-Fig. 4(C) are cross section views along line [[X-X']] 4-4 shown in Fig. 5. In this embodiment, elements which correspond to the elements mentioned above are marked with the same symbols.

Please replace the abstract with the following amended abstract:

A semiconductor device includes a first wall and a second wall. The first wall is arranged in a pad region which surrounds a chip region, and the second wall is arranged on a semiconductor chip mounted in the chip region. Conductive lines are arranged between the first wall and the second wall and are encapsulated by [[a]] an encapsulating material formed between the first and second walls.